REMARKS

In accordance with the foregoing, claim 1 has been amended to include the respective limitations of dependent claims 2, 6 and 7 which are cancelled.

Similarly, claim 8 has been amended to include the respective limitations of dependent claims 10 and 11 which are cancelled.

Claims 3 and 4 have been amended to depend from claim 1.

Claims 10 and 11 are cancelled, without prejudice.

Accordingly, claims 1, 3-5, 8 and 9 remain pending herein.

Further, a corrected formal drawing of Fig. 4 is supplied herewith, correcting a typographical error therein.

No new matter is presented and, accordingly, approval and entry of the amended claims and the corrected formal Fig. 4 are respectfully requested.

Item 3: Rejection of Claims 1-11 for anticipation under 35 U.S.C. 102(b) by Beausang et al. (USP'692).

Items 4 through 10 address selected groups of claims otherwise grouped together in the rejection of Item 3. The rejections of all are respectfully traversed.

As to the rejection of claims 1 and 8 in Item 4, Applicants respectfully submit that the cited portions of Beausang et al. relied upon in support of the rejection are simply wide of the mark and do not support a rejection those independent claims as originally filed --much less, as those claims have now been amended as hereinabove referenced.

The Invention As Claimed

According to claim 1, as amended above, the scan flip-flops for the scan chain are not registered in the layout library, and instead, the scan flip-flops are expanded by the standard cells that are registered in the layout library. Therefore, the registration of the scan flip-flops to the layout library is not necessary and the expansion of the scan flip-flops to standard cells allows the optimization of the layout through the automatic layout process. However, if the chain order of scan flip-flops is reordered in the automatic layout process, since the scan flip-flops are already expanded to standard cells, the test pattern data cannot be generated by the

test pattern generation tool. That is, the test pattern generation tool generates test pattern data from a netlist having scan flip-flops as softmacros --and it is difficult for the test pattern generation tool to generate a test pattern from a net list having scan flip-flops that are already expanded to standard cells.

Therefore, in the present invention, flip-flops in the netlist NL1 (see Fig. 4) are converted into scan flip-flops (softmacros) for the netlist NL4 according to the order of the recorded scan flip-flops. Then, the test pattern data F12 is generated from the netlist NL4. After that, the scan fillip-flops of the netlist NL4 are expanded to standard cells to produce the final netlist NL5.

Thus, in the present invention, since scan Flip-flops are not registered in the layout library, once the expanded netlist NL3 is laid out and the scan chain order is reordered for optimization, the test pattern generation is difficult. Therefore, the original netlist NL1 is converted into the netlist NL4 according to the reordered scan chain order, and the test pattern is generated from the netlist NL4 having scan flip-flops as softmacros.

The Disclosure of Beausang et al. USP'692

As noted above, Beausang et al. is altogether remote from the invention as defined in claim 1 as amended herein. The reference discloses an analyzing step for generating a scan plan based on the design and a synthesizing step for synthesizing the scan plan within the design by inserting scan resources into the design to realize the number of balanced top level scan chains of the scan plan. In the analyzing step, there are various methods to generate the scan plan.

Figs. 6-12 show various methods to generate the scan plans for the circuit design. According to the disclosure of these figures, there is only an explanation of processing at the scan flip-flop level; there is no disclosure of any expansion of scan flip-flops to standard cells, of layout of the standard cells, of the reorder of the scan chain at the layout process, and of the test pattern generation from a newly generated netlist derived from the original netlist according to the reordered scan chain order.

The Reading of Claim 1 in Item 4 of the Action on Beausang et al. is without basis

While the recitations of claim 1 (as originally filed) are set forth in Item 4, the purported reading thereof on the disclosure of the reference is without basis. An electronic scan of the specification of Beausang et al. reveals it has no disclosure of any numerous, significant recitations of claims 1 and 8, such as "convert", "flip-flops" "reorder" "standard" (cell), "expansion...." and the like.

The Examiner sets forth specific citations of:

(1) Figures 6-14 and column 10, line 54 to column 11, lines 39;

(2) Figures 6-14 and column 11, line 39 to column 13, line 19;

(3) Fig. 1 and 6-14 and column 13, line 21 to column 14 line 40; and

(4) Fig. 1 and 6-14 and column 11, line 21 to column 14 line 40 and background

In citation (1) there is no reference to flip-flops, much less to the recited flip-flops of claims 1 and 8.

Citation (2) has only a brief --and irrelevant-- reference to flip-flops, at column 13, lines 13-14: "Scan styles include mixed, multiplexed flip-flop."

Citation (3) likewise includes only a brief --and irrelevant-- reference to flip-flops, at column 14 line 13-17, relating to input and output connections.

Citation (4) is merely a replication of the combination of citations 2 and 3 and the same comments apply.

The Invention Defined By Claim 8 Is Significantly Different From That Defined By Claim 1

The invention of claim 8 (as amended) relates to the logic optimization step form the netlist NL4, having the scan Flip-flops as sotfmacro, to the netlist NL5 having the expanded standard cells. In the optimization step, the standard cells are substituted for a different standard cell, as shown in Fig. 10 in the present specification. There is no disclosure of this invention in the cited reference.

Dependent Claims

The dependent claims 3, 4, 5 and 9 inherit the limitations of their respective independent claims 1 and 8 and are submitted to patentably distinguish over Beausang et al. for at least the same reasons.

Conclusion

In accordance with the foregoing, it is respectfully submitted that the pending claims patentably distinguish over the reference of record, and, there be no other objections or rejections, that the application is in condition for allowance, which action is earnestly solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: Sept. 16, 2004

By: _____
H. J. Staas
Registration No. 22,010

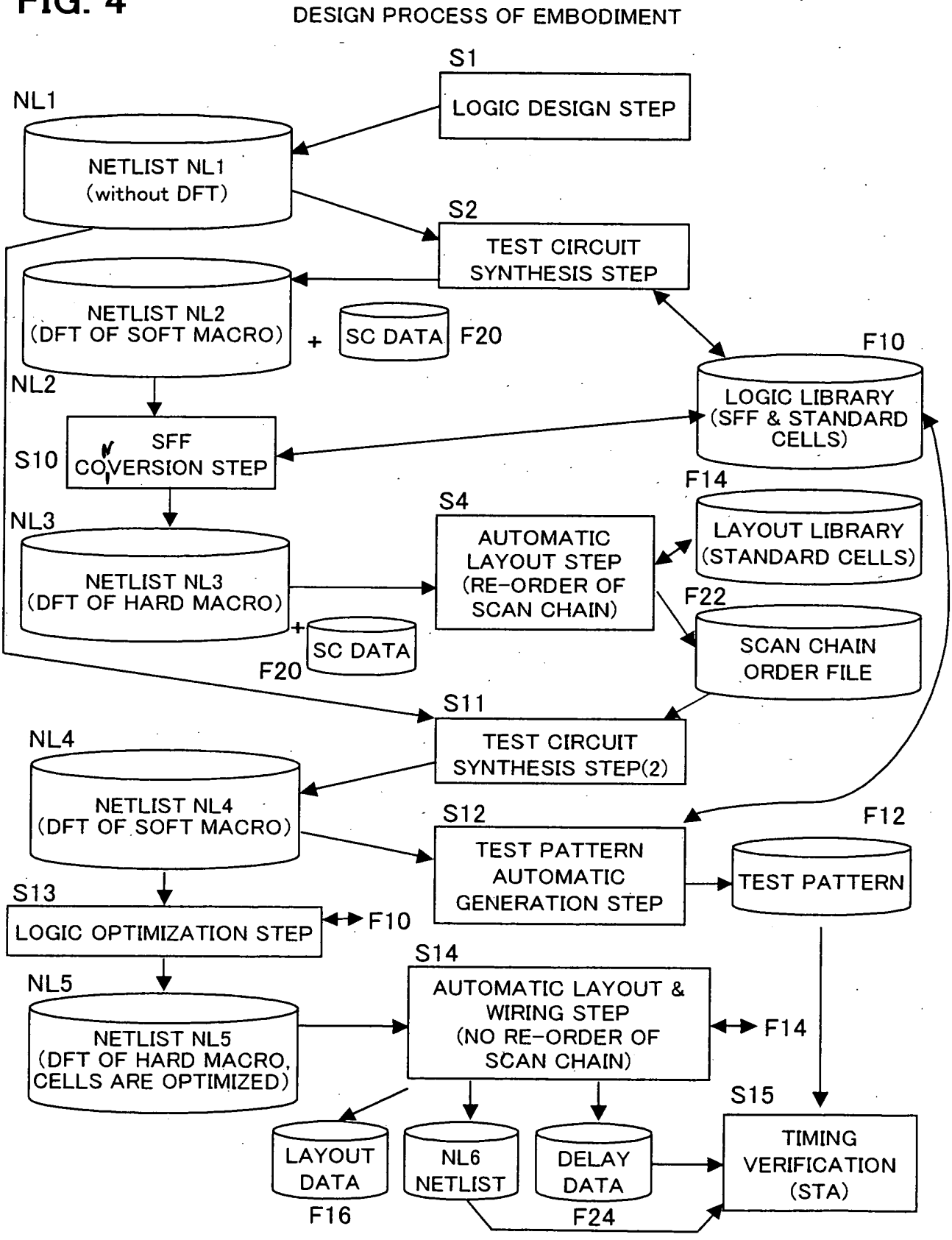
1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

AMENDMENTS TO THE DRAWINGS:

In rectangular block designated "S10", correct the spelling of "coversion" to --conversion--

A corrected formal drawing corresponding red ink marked copy showing the correction is filed herewith.

FIG. 4


DESIGN PROCESS OF EMBODIMENT
S1
LOGIC DESIGN STEP
NL1
NETLIST NL1
(without DFT)
S2
TEST CIRCUIT
SYNTHESIS STEP
NETLIST NL2
(DFT OF SOFT MACRO)
+
SC DATA
F20
F10
NL2
LOGIC LIBRARY
(SFF & STANDARD
CELLS)
S10
SFF
CONVERSION STEP
F14
S4
NL3
AUTOMATIC
LAYOUT STEP
(RE-ORDER OF
SCAN CHAIN)
LAYOUT LIBRARY
(STANDARD CELLS)
NETLIST NL3
(DFT OF HARD MACRO)
F22
+
SC DATA
SCAN CHAIN
ORDER FILE
F20
S11
TEST CIRCUIT
SYNTHESIS STEP(2)
NL4
NETLIST NL4
(DFT OF SOFT MACRO)
S12
F12
TEST PATTERN
AUTOMATIC
GENERATION STEP
TEST PATTERN
S13
LOGIC OPTIMIZATION STEP
F10
S14
NL5
AUTOMATIC LAYOUT &
WIRING STEP
(NO RE-ORDER OF
SCAN CHAIN)
F14
NETLIST NL5
(DFT OF HARD MACRO,
CELLS ARE OPTIMIZED)
S15
LAYOUT
DATA
NL6
NETLIST
DELAY
DATA
TIMING
VERIFICATION
(STA)
F16
F24